

DECLARATION

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled "MEMORY MODULE HAVING INTERCONNECTED AND STACKED INTEGRATED CIRCUITS," the specification of which:

- ☒ is attached hereto.
☐ was filed on _____ as Application Serial No. _____
 and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability of the subject matter claimed in this application, as "materiality" is defined in 37 C.F.R. § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate listed below, or under § 365(a) of any PCT international application listed below designating least one country other than the United States of America, and have identified below any foreign application for patent or inventor's certificate, or of any PCT international application, having a filing date before that of the application on which priority is claimed.

<u>Prior Foreign Application No.</u>	<u>Country</u>	<u>Filing Date</u> <u>(mm/dd/yy)</u>	<u>Priority</u> <u>Claimed</u>	<u>Cert. copy</u> <u>Attached</u>
N/A				

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

<u>Provisional Application No.</u>	<u>Filing Date</u> <u>(mm/dd/yy)</u>
N/A	


I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) listed below, or under § 365(c) of any PCT international application listed below designating the United States of America, and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in 37 C.F.R. § 1.56, which became available between the filing date of the prior application and the national or PCT international filing date of this application.

<u>Parent Application No.</u>	<u>Filing Date</u> <u>(mm/dd/yy)</u>	<u>Parent Patent No. (if applicable) or Status</u>
N/A		

10080036-021902

I hereby declare that all statements made herein of my own knowledge are true and that all statements made herein on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

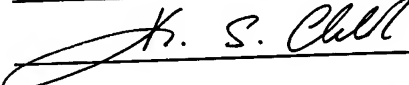
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Inventor's Signature:  Date: 2/13/02

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Inventor's Full Name: Khushrav S. Chhor

Inventor's Signature:  Date: 2/14/02

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(Include number, street name, city, state and zip code)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:
Verma, et al.

Filed: Herewith

Serial No. Unknown

For: MEMORY MODULE HAVING
INTERCONNECTED AND STACKED
INTEGRATED CIRCUITS

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Attorney Dkt. No. 5732-00300

POWER OF ATTORNEY BY ASSIGNEE

Under the provisions of 37 C.F.R. § 3.71, the undersigned assignee of record of the entire interest in the above-identified patent/patent application by virtue of an assignment recorded (check as applicable):

☒
☐
☐

Concurrently herewith

Date Recorded

Reel _____ Frame _____

I elect to conduct the prosecution of the application/maintenance of the patent to the exclusion of the inventor(s). The undersigned hereby declares that he has reviewed the above-referenced assignment and hereby declares that, to the best of his knowledge, title is in the Assignee, and further declares that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true. The assignee hereby revokes any previous powers of attorney and appoints the following to prosecute this application/maintain this patent and transact all business in the Patent and Trademark Office connected therewith:

Liza K. Toth, Reg. No. 31,065 of Matrix Semiconductor, Inc.
Kevin L. Daffer, Reg. No. 34,146; B. Noel Kivlin, Reg. No. 33,929; Eric B. Meyertons, Reg.
No. 34,876; and Gentry E. Crook, Reg. No. 44,633 of Conley, Rose & Tayon LLP

Please direct all communications to: Conley, Rose & Tayon, P. O. Box 398, Austin, Texas 78767,
Tel. No.: (512) 476-1400, to the attention of: Kevin L. Daffer

ASSIGNEE
MATRIX SEMICONDUCTOR, INC.

Date: 2/14/02

BY: Liza K. Toth
Liza K. Toth, VP, Intellectual Property

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